CLAIMS

What is claimed is:

1. A method for parallel generating channelization codes, such as Walsh-Hadamard (WH) channelization codes and Orthogonal Variable Spreading Factor (OVSF) channelization codes, said channelization codes being formed by a plurality of strings of antipodal digits, each having a length L and being identifiable by respective indices I formed by strings of binary digits, each having a length N equal to a logarithm in base two of the length L of said channelization codes, the antipodal digits of said channelization codes being able to assume values +1 and -1 and the binary digits of said indices I being able to assume values 0 and 1, said method comprising:

determining the antipodal digits of said channelization codes according to the binary digits of the corresponding indices I by implementing the following:

a) determining intermediate binary digits:

$U_0 = X$

$U_i = U_{i-2^k} \oplus I_{Bk}$

where:

$1 \leq i \leq 2^N-1$

$k = INT[\log_2 i]$, $0 \leq k \leq N-1$

I_{Bk} are the binary digits of the indices I of said channelization codes,

X is a binary encoding digit, a value of which depends upon a type of binary encoding chosen for the antipodal digits of the channelization codes, and

$\oplus$ represents logic operation EXOR; and

b) encoding said intermediate binary digits with respective antipodal digits of said channelization codes according to said binary encoding digit X, said encoding being performed using a criterion according to which intermediate binary digits 0 and 1 are encoded, respectively, with antipodal digits -1 and +1 if the binary encoding digit X is equal to 1, whilst they are encoded with antipodal digits +1 and -1 if the binary encoding digit X is equal to 0.

2. The method according to claim 1 wherein the binary digits I_{Bk} of the indices I of the WH channelization codes range, as k increases from 0 to N-1, from a least significant bit to a most significant bit.

3. The method according to claim 1 wherein the binary digits I_{Bk} of the indices I of the OVSF channelization codes range, as k increases from 0 to N-1, from a most significant bit to a least significant bit.

4. A low consumption device for parallel generating channelization codes for CDMA transmissions, such as Walsh-Hadamard (WH) channelization codes and Orthogonal Variable Spreading Factor (OVSF) channelization codes, said channelization codes being formed by a plurality of strings of antipodal digits, each having a length L and being identifiable by respective indices I formed by strings of binary digits, each having a length N equal to a logarithm in base two of the length L of said channelization codes, the antipodal digits of said channelization codes being able to assume values +1 and -1 and the binary digits of said indices I being able to assume values 0 and 1, said device comprising:

processing means for determining the antipodal digits of said channelization codes according to the binary digits of the corresponding indices I, said processing means including:

a) computation means for receiving the binary digits I_{Bk}, with $0 \leq k \leq N-1$, of the indices I of said channelization codes and a binary encoding digit X, a value of which depends upon a type of binary encoding chosen for the antipodal digits of the channelization codes, and for supplying intermediate binary digits:

$$U_0 = X$$

$$U_i = U_{i-2^k} \oplus I_{Bk}$$

where:

$$1 \leq i \leq 2^N-1$$

$$k = INT[\log_2 i],\ 0 \leq k \leq N-1$$

⊕ represents EXOR logic operation; and

b) encoding means for encoding said intermediate binary digits with respective antipodal digits of said channelization codes according to said binary encoding digit X, said encoding being performed using a criterion according to which intermediate binary digits 0 and 1 are encoded, respectively, with antipodal digits -1 and +1 if the binary encoding digit X is equal to 1, whilst they are encoded with antipodal digits +1 and -1 if the binary encoding digit X is equal to 0.

5. The device according to claim 4 wherein the binary digits I_{Bk} of the indices I of the WH channelization codes range, as k increases from 0 to N-1, from a least significant bit to a most significant bit.

6. The device according to claim 4 wherein the binary digits I_{Bk} of the indices I of the OVSF channelization codes range, as k increases from 0 to N-1, from a most significant bit to a least significant bit.

7. A device to parallel-generate first and second types of channelization codes for transmission, the channelization codes being formed by a plurality of strings of antipodal digits, each having a length L and being identifiable by respective indices I formed by strings of binary digits, each having a length N equal to a logarithm in base two of the length L of the channelization codes, the antipodal digits of the channelization codes being able to assume values +1 and -1 and the binary digits of the indices I being able to assume values 0 and 1, the device comprising:

a processor to determine the antipodal digits of the channelization codes according to the binary digits of the corresponding indices I, the processor having:

a) a computation unit to receiving the binary digits I_{Bk}, with $0 \leq k \leq N-1$, of the indices I of the channelization codes and a binary encoding digit X, a value of which is based at least in part upon a type of binary encoding chosen for the antipodal

digits of the channelization codes, the computation unit able to supply intermediate binary digits:

$$U_0 = X$$

$$U_i = U_{i-2^k} \oplus I_{Bk}$$

where:

$$1 \leq i \leq 2^N-1$$

$$k = INT[\log_2 i],\ 0 \leq k \leq N-1$$

$\oplus$ represents a logic operation; and

b) an encoder unit coupled to the computation unit to encode the intermediate binary digits with respective antipodal digits of the channelization codes according to the binary encoding digit X, the encoder unit able to perform the encoding based on a criterion according to which intermediate binary digits 0 and 1 are encoded, respectively, with antipodal digits -1 and +1 if the binary encoding digit X is equal to 1, and the intermediate binary digits are encoded with antipodal digits +1 and -1 if the binary encoding digit X is equal to 0.

8. The device of claim 7 wherein the first and second types of channelization codes respectively comprise Walsh-Hadamard-like and Orthogonal Variable Spreading Factor-like codes.

9. The device of claim 7 wherein the transmission comprises a code division multiple access (CDMA)-like transmission.

10. The device of claim 7 wherein the binary digits I_{Bk} of the indices I of the first type channelization codes range, as k increases from 0 to N-1, from a least significant bit to a most significant bit.

11. The device of claim 7 wherein the binary digits I_{Bk} of the indices I of the second type of channelization codes range, as k increases from 0 to N-1, from a most significant bit to a least significant bit.

12. The device of claim 7 wherein either one or both of the computation unit and encoder unit include a plurality of dual-input logic gates, some of which are coupled to receive a reference voltage on a first input terminal and a value of one of the indices I on a second input terminal.

13. The device of claim 12 wherein the logic gates are coupled to perform the logic operation, which comprises an EXOR operation.

14. The device of claim 12 wherein the reference voltage comprises ground.

15. The device of claim 12 wherein the reference voltage comprises a voltage from a voltage supply.

16. The device of claim 12 wherein the logic gates are coupled to provide respective binary digits U_i at their output terminals.